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Presented for filing is a new original patent application of:

Applicant: SHUICHI KIKUCHI AND YUMIKO AKAISHI

Title: SEMICONDUCTOR DEVICE AND METHOD OF
MANUFACTURING THE SAME

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Enclosed are the following papers, including those required to receive a filing date under 37 CFR 1.53(b):

	Pages
Specification	28
Claims	12
Abstract	1
Declaration	4
Drawing(s)	22

Enclosures:

- Assignment cover sheet and an assignment, 3 pages, and a separate \$40 fee.
- A certified copy of the priority application will be filed at a later date.
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Under 35 USC 119, this application claims the benefit of foreign priority applications filed in Japan, serial numbers Hei. 10-335877, Hei. 10-345651 and Hei. 10-351779, filed November 26, 1998, December 4, 1998 and December 10, 1998, respectively.

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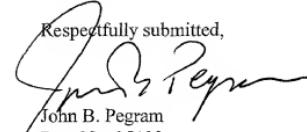
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APPLICATION
FOR
UNITED STATES LETTERS PATENT

TITLE: SEMICONDUCTOR DEVICE AND METHOD OF
MANUFACTURING THE SAME

APPLICANT: SHUICHI KIKUCHI AND YUMIKO AKAISHI

SEARCHED = 6/20/99

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SEMICONDUCTOR DEVICE
AND METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE ART

5 1. Technical Field

The present invention relates to a semiconductor device and a method of manufacturing the same and, more particularly, a technology for an LD (Lateral Double Diffused) MOS transistor as a high voltage element employed in a liquid crystal driving IC, etc.,

10 for example.

2. Related Art of the Invention

In the LDMOS transistor structure, a new diffusion region is formed by diffusing a different conductivity type impurity into a diffusion region formed on the surface side of a semiconductor substrate, and then a difference in lateral diffusion lengths of these diffusion regions is utilized as an effective channel length. Thus, since a short channel can be formed, the LDMOS transistor is suitable for the low ON-resistance device.

FIG.18 is a sectional view showing the LDMOS transistor in the prior art. The N-channel LDMOS transistor structure is shown as an example. In this case, although explanation of the P-channel LDMOS transistor structure is omitted, it is well known that the P-channel LDMOS transistor structure has the similar structure except for the different conductivity type.

In FIG.18, 1 denotes one conductivity type, e.g., P-type semiconductor substrate, and 2 denotes an N-type well region. A P-type body region 3 is formed in the N-type well region 2, and then an N-type diffusion region 4 is formed in the P-type body region

3. An N-type diffusion region 5 is also formed in the N-type well region 2. A gate electrode 7 is formed on a gate insulating film 6 on the surface of the substrate. A channel region 8 is formed on a surface region of the P-type body region 3 immediately below the gate electrode 7.

Then, the N-type diffusion region 4 acts as a source region, the N-type diffusion region 5 acts as a drain region, and the N-type well region 2 located under a LOCOS oxide film 9A acts as a drift region. Then, 10 and 11 denote a source electrode and a drain electrode respectively, 12 denotes a P-type diffusion region for supplying the potential to the P-type body region 3, and 13 denotes an interlayer insulating film.

In the above LDMOS transistor, since the N-type well region 2 is formed by diffusing the impurity, the impurity concentration of the surface of the N-type well region 2 is increased. Thus, the current is ready to flow through the surface of the N-type well region 2, and also the higher breakdown voltage can be achieved. Then, the LDMOS transistor having such configuration is called a REduced SRface (RESURF) type LDMOS, and a dopant concentration in the drift region of the N-type well region 2 is set to satisfy RESURF conditions. Such technology is disclosed in JPA (Patent Application Publication (KOKAI) Hei) 9-139438, etc.

However, as shown in FIG.18, since the N-type well region 2 is formed uniformly up to the same depth position, it prevents the higher breakdown voltage and the reduction in ON-resistance.

In addition, as shown in FIG.20, in the case that a plurality of LDMOS transistors having the above structure are arranged via a element isolation film 9B, the element isolation films 9B to

isolate the adjacent transistors are increased in size to thus prevent the higher integration. In other words, the N-type well regions 2 which are positioned adjacently via the element isolation film 9B have the large lateral spread since they are formed by the well-known well diffusion step, and also the depletion layer widely spreads. Hence, the element isolation film 9B needs an L2 (about 10 μm to 30 μm) size, for example.

Further, as shown in FIG.19A, there is provided a device constituted by the P-channel high breakdown voltage MOS transistor (Pch MOS Tr) and the N-channel LDMOS transistor (Nch DMOS Tr) as a CMOS circuit which can achieve the high breakdown voltage. In this case, as shown in FIG.19B, in the P-channel high breakdown voltage MOS transistor, an N-type well region 51 is formed on a one conductivity type, e.g., P-type semiconductor substrate 1, then a gate electrode 57 is formed on a surface of the N-type well region 51 via a gate insulating film 56, then P-type low concentration diffusion regions 54A, 54B are formed on a substrate surface layer to be adjacent to the gate electrode 57, and then P-type high concentration diffusion regions 55A, 55B are formed in the P-type diffusion regions 54A, 54B. The P-type diffusion regions 54A, 55A act as a source region, and the P-type diffusion regions 54B, 55B act as a drain region.

Then, the CMOS structure is constructed by such P-channel high breakdown voltage MOS transistor and the foregoing N-channel LDMOS transistor.

However, in the CMOS structure in the prior art the process for manufacturing the N-channel LDMOS transistor cannot be sufficiently used.

Summary of the Invention

Therefore, a first object of the present invention is to provide a semiconductor device which is responsible to requests for the higher breakdown voltage and the reduction in its ON-resistance, 5 and a method of manufacturing the same.

Therefore, a second object of the present invention is to provide a semiconductor device which is responsible to requests for the higher breakdown voltage and the reduction in its ON-resistance and also enables the higher integration density, and a method of 10 manufacturing the same.

Therefore, a third object of the present invention is to provide a semiconductor device which makes it possible to improve the characteristics of the P-channel high breakdown MOS transistor by using practically and sufficiently fabrication processes for the 15 N- channel LDMOS transistor without causing the increase in the number of manufacturing steps, and a method of manufacturing the same.

Accordingly, in order to achieve the above first object, as shown in Fig.1, the present invention is characterized by providing 20 a semiconductor device, for example, an N-channel LDMOS transistor, which comprises a source region 4, a channel region 8, and a drain region 5, and a gate electrode 7 formed on the channel region 8, and a drift region formed between the channel region 8 and the drain region 5, wherein an N-type low concentration layer 22 serving as 25 the drift region is formed shallowly at least below the gate electrode 7 (first N-type layer 22A) but formed deeply in a neighborhood of the drain region 5 (second N-type layer 22B).

In this manner, a RESURF effect can be improved by forming

the drift region shallowly under the gate electrode 7.

Then, as shown in Fig.2A, a method of manufacturing the semiconductor device of the present invention comprises following steps. Two kind N-type impurities (for example, arsenic ion and phosphorus ion) are ion-implanted to form an N⁻type layer 22 serving as a drift region in a P-type well region 21 in a P-type semiconductor substrate 1. Then, as shown in Fig.2B, a LOCOS oxide film 9 is formed by oxidizing selectively a certain region on the substrate 1, and the N⁻type low concentration layer 22A, 22B is formed at a 5 relatively deep position in the P-type well region 21 and on a surface layer of the substrate 1 by using a difference in diffusion coefficients of the arsenic ion and the phosphorus ion respectively. Then, as shown in Fig.3A, a P-type impurity (for example, boron ion) is ion-implanted and diffused into the surface layer of the 10 substrate 1 in a source forming region by using a photoresist film 39 which is formed on a drain forming region on the substrate 1 as a mask so as to cancel the N⁻type layer 22B formed at the relatively deep position in the P-type well region 21 in the source forming 15 region by a diffusion of the boron ion.

Then, as shown in Fig.3B, a gate insulating film 6 is formed on the substrate 1, then a gate electrode 7 is formed to extend from the gate insulating film 6 to the LOCOS oxide film 9, and then as shown in Fig.4A, a P-type body region 3 is formed adjacently to one end portion of the gate electrode 7 by implanting and diffusing the 20 P-type impurity (for example, boron ion) by using a photoresist film 40 which is formed to cover the gate electrode 7 and the drain forming region as a mask. Then, as shown in Figs.4B and 5A, an N-type 25 diffusion region 4, 5 serving as a source/drain region is formed

by implanting the N-type impurities (for example, phosphorus ion and arsenic ion) into the source forming region and the drain forming region formed in the P-type body region 3 by using a photoresist film 41,44 as a mask.

5 Further, in order to achieve the above second object, the present invention is characterized by providing a semiconductor device, for example, as shown in Fig.8, the N-channel LDMOS transistor, comprising a plurality of parallel-aligned structures, each of which including a source region 4, a channel region 8, and
10 a drain region 5, and a gate electrode 7 formed on the channel region 8, and an N⁻-type layer 22 (drift region) which is formed shallowly at least below the gate electrode 7 between the channel region 8 and the drain region 5 (first N⁻-type layer 22A) but formed deeply in a neighborhood of the drain region 5 (second N⁻-type layer 22B),
15 via a element isolation film 9B, wherein a channel stopper layer 38 is formed under the element isolation film 9. As a result, improvement of the RESURF effect and the higher integration can be achieved by forming the drift region shallowly under the gate electrode 7.

20 Then, a method of manufacturing a semiconductor device of the present invention comprises following steps as shown in Fig.9 as an embodiment. Two kind N-type impurities (for example, arsenic ion and phosphorus ion) are ion-implanted to form the N⁻-type layer 22 serving as the drift region in the P-type well region 21 in the
25 P-type semiconductor substrate 1. Then, as shown in Fig.10, a silicon nitride film 34 serving as a mask in LOCOS-oxidizing via postprocessing is formed on the substrate 1, and then the P-type impurity (for example, boron ion) is ion-implanted into a surface

of the substrate by using a photoresist film 36 which is formed to cover the silicon nitride film 34 as a mask as shown in Fig.11. Then, a first LOCOS oxide film 9A and a second LOCOS oxide film 9B are forming by oxidizing selectively certain regions on the substrate

- 5 by using the silicon nitride film 34 as a mask, and the N⁻-type low concentration layer 22A, 22B is formed at a relatively deep position in the P-type well region 21 and on a surface layer of the substrate 1 respectively by using a difference in diffusion coefficients of two kind N-type impurities (for example, arsenic ion and phosphorus ion), and then a channel stopper layer 38 is formed under the second LOCOS oxide film 9B. Then, as shown in Fig.12, the first conductivity type impurity is ion-implanted and diffused into the surface layer of the substrate 1 in the source forming region by using a photoresist film 39 which is formed in the drain forming region on the substrate 1 as a mask so as to cancel the N⁻-type layer 22B formed at the relatively deep position in the P-type well region 21 in the source forming region by the diffusion of the boron ion. Then, as shown in Fig.13, the gate insulating film 6 is formed on the substrate 1, then the gate electrode 7 is formed so as to extend
- 10 from the gate insulating film 6 to the first LOCOS oxide film 9A, and then the P-type body region 3 is formed adjacently to one end portion of the gate electrode 7 by implanting and diffusing the P-type impurity by using a photoresist film 40 which is formed to cover the gate electrode 7 and the drain forming region as a mask.
- 15 Then, as shown in Fig.16, an N-type diffusion region 4, 5 serving as the source/drain region is formed by implanting the N-type impurities (for example, phosphorus ion and arsenic ion) into the source forming region and the drain forming region formed in the

P-type body region 3 by using a photoresist film 42 as a mask (Fig. 15).

Further, in order to achieve the above third object, as shown in Fig.5, the present invention is characterized by providing a semiconductor device which includes an N -channel $DMOS$ transistor

5 (A) having a source region 4, a channel region 8, a drain region
5, a gate electrode 7 formed on the channel region 8, and a drift
region formed of an N-type layer 22 between the channel region 8
and the drain region 5, and a P-channel high breakdown voltage MOS
transistor (B) having a source region 54, a channel region 58, a
10 drain region 55, and a gate electrode 57 formed on the channel region
58, wherein the drift region (N-layer 22) in the N-channel LDMOS
transistor (A) is formed shallowly at least below the gate electrode
7 (first N-type layer 22A) but formed deeply in a neighborhood of
the drain region 5 (second N-type layer 22B). In addition, a
5 source/drain region 54, 55 of the P-channel high breakdown voltage
MOS transistor (B) consists of a low concentration source/drain
region 54A, 55A, a high concentration source/drain region 54B, 55B,
and a middle concentration source/drain region 54C, 55C.

20 Moreover, as shown in Fig.2A, a method of manufacturing the semiconductor device of the present invention comprises following steps. A photoresist film 31 which has an opening portion 31a over a part of a P-type well region 21 on a P-type semiconductor substrate 1 on which the P-type well region 21 and an N-type well region 51
25 is formed, and then two kind second conductivity type impurities (for example, arsenic ion and phosphorus ion) having a different diffusion coefficient are ion-implanted by using the photoresist film 31 as a mask. Then, as shown in Fig.2B, a silicon nitride film

34 is formed in a certain region on the substrate 1, then a LOCOS oxide film 9 is formed by oxidizing selectively the substrate 1 by using the silicon nitride film 34 as a mask, and N-type layers 22B, 22A are formed at a relatively deep position in the P-type well region 21 and on a surface layer of the substrate 1 by using a difference in diffusion coefficients of two kind N-type impurities respectively. Then, as shown in Fig.3A, a P-type impurity (for example, boron ion) is ion-implanted and diffused into a source forming region in the P-type well region 21 and the surface layer 10 of the substrate 1 in a source/drain forming region in the N-type well region 51 by using a photoresist film 39 which has opening portions 39a over the source forming region in the P-type well region 21 and the source/drain forming region in the N-type well region 51 as a mask so as to cancel the N-type layer 22B formed at the 15 relatively deep position in the source forming region in the P-type well region 21 by a diffusion of the boron ion and to form a P-type low concentration source/drain region 54A, 55A. Then, as shown in Fig.3B, a first gate insulating film 6 is formed in a region other than the LOCOS oxide film 9 on the P-type well region 21, then 20 a second gate insulating film 56 is formed in a region other than the LOCOS oxide film 9 on the N-type well region 51, and then a first gate electrode 7 and a second gate electrode 57 are formed on the first gate insulating film 6 and the second gate insulating film 56 respectively. Then, as shown in Fig.4A, the first conductivity 25 type impurity (for example, boron ion) is ion-implanted and diffused by using a photoresist film 40 which covers the first gate electrode 7 in the P-type well region 21 and the drain forming region and has an opening portion 40a over a part of the source/drain forming region

on the N-type well region 51 as a mask, so as to form a P-type body region 3 adjacently to one end portion of the first gate electrode 7 and to form a P-type middle concentration source/drain region 54C, 55C in a region separated from the second gate electrode 57. Then,
5 as shown in Fig.4B, an N-type low concentration source region 4A is formed by ion-implanting the N-type impurity (for example, phosphorus ion) by using a photoresist film 41 which has an opening portion 41a located over the source forming region in the P-type well region 21 as a mask. Then, sidewall spacer films 43 are formed
10 on side wall portions of the first gate electrode 7 and the second gate electrode 57, and then as shown in Fig.5A an N-type high concentration source/drain region 4B, 5B is formed by ion-implanting the N-type impurity (for example, arsenic ion) by using a photoresist film 44 which having an opening portion 44a located
15 over the source/drain forming region in the P-type well region 21 as a mask. Then, as shown in Fig.5B a P-type high concentration source/drain region 54B, 55B is formed by implanting the P-type impurity (for example, boron difluoride ion) by using a photoresist film 45 having at least an opening portion 45a which is located over
20 the N-type well region 51 and is smaller than at least the P-type middle concentration source/drain region 54C, 55C as a mask.

Brief Description of the Drawings

FIG.1 is a sectional view showing a semiconductor device manufacturing method according to a first embodiment of the present
25 invention;

FIGS.2A and 2B are sectional views showing a semiconductor device manufacturing method according to the first embodiment of the present invention;

FIGS.3A and 3B are sectional views showing a semiconductor device manufacturing method according to the first embodiment of the present invention;

5 FIGS.4A and 4B are sectional views showing a semiconductor device manufacturing method according to the first embodiment of the present invention;

FIGS.5A and 5B are sectional views showing a semiconductor device manufacturing method according to the first embodiment of the present invention;

10 FIG.6 is a graph showing a concentration distribution of various ions for the purpose of illustration of the drift region forming principle;

FIG.7 is a sectional view showing a semiconductor device manufacturing method according to a second embodiment of the present invention;

15 FIG.8 is a sectional view showing a semiconductor device manufacturing method according to a third embodiment of the present invention;

FIG.9 is a sectional view showing a semiconductor device manufacturing method according to the third embodiment of the present invention;

20 FIG.10 is a sectional view showing a semiconductor device manufacturing method according to the third embodiment of the present invention;

25 FIG.11 is a sectional view showing a semiconductor device manufacturing method according to the third embodiment of the present invention;

FIG.12 is a sectional view showing a semiconductor device

manufacturing method according to the third embodiment of the present invention;

FIG.13 is a sectional view showing a semiconductor device manufacturing method according to the third embodiment of the present invention;

FIG.14 is a sectional view showing a semiconductor device manufacturing method according to the third embodiment of the present invention;

FIG.15 is a sectional view showing a semiconductor device manufacturing method according to the third embodiment of the present invention;

FIG.16 is a sectional view showing a semiconductor device manufacturing method according to the third embodiment of the present invention;

FIG.17 is a sectional view showing a semiconductor device manufacturing method according to a fourth embodiment of the present invention;

FIG.18 is a view showing a semiconductor device in the prior art;

FIGS.19A and 19B are views showing the semiconductor device in the prior art;

FIG.20 is a view showing the semiconductor device in the prior art;

FIG.21 is a graph showing a relation between a clamp voltage and an acceptor concentration; and

FIG.22 is a view showing a relation between a concentration of a junction portion of a shallow N-layer and a thickness of a depletion layer caused in the first embodiment of the present

invention.

Description of the preferred Embodiment

A semiconductor device and a method of manufacturing the same according to a first embodiment of the present invention will be 5 explained with reference to the accompanying drawings hereinafter.

FIG.1 is a sectional view showing the semiconductor device and the method of manufacturing the same according to the first embodiment of the present invention. A configuration consisting of the N-channel LDMOS transistor (A) and the P-channel high 10 breakdown voltage MOS transistor (B) is shown as an example. In this case, same symbols are affixed to constituent elements similar to those in the prior art, and their explanation will be simplified.

In FIG.1, 1 denotes one conductivity type, e.g., P-type semiconductor substrate, and 21 denotes a P-type well region. An 15 N⁻ type layer 22 as well as the P-type body region (PB) 3 is formed in the P-type well region 21. The N-type diffusion region 4 is formed in the P-type body region 3, and the N-type diffusion region 5 is also formed in the N⁻ type layer 22. The gate electrode 7 is formed on the surface of the substrate via the gate insulating film 20 6. The channel region 8 is formed on the surface region of the P-type body region 3 immediately below the gate electrode 7.

Then, the N-channel LDMOS transistor (A) is constructed in which the N-type diffusion region 4 acts as the source region, the N-type diffusion region 5 acts as the drain region, and the N⁻ type layer 22 located under the LOCOS oxide film 9 acts as the drift 25 region. The P-type diffusion region 12 for supplying the potential to the P-type body region 3 is formed adjacently to the N-type diffusion region 4. The N⁻ type layer 22 formed in the P-type well

region 21 is formed shallowly below the gate electrode 7 (first N-type layer 22A) and is formed deeply in the neighborhood of the N-type diffusion region (drift region) 5 (second N-type layer 22B). According to such configuration, the higher breakdown voltage and the lower ON-resistance of the N-channel LDMOS transistor (A) can be achieved. More particularly, since the concentration of the first N-type layer 22A being formed shallowly below the gate electrode 7 is set high, the ON-resistance can be reduced and also the current flow can be made easy. While, since the concentration of the second N-type layer 22B being formed in the neighborhood (drift region position) of the N-type diffusion region (drift region) 5, the depletion layer can be easily extended and also the high breakdown voltage can be achieved (see the concentration distribution shown in FIG.6). The N-channel LDMOS transistor of the first embodiment has the breakdown voltage of about 30 V.

Then, 51 denotes an N-type well region. A gate electrode 57 is formed on a surface of the substrate over the N-type well region 51 via a gate insulating film 56. A channel region 58 is formed in a surface region immediately below the gate electrode 57. Then, 20 P-type diffusion regions 54, 55 are formed to be adjacent to the gate electrode 57. The P-channel high breakdown voltage MOS transistor (B) using the P-type diffusion region 54 as the source region and the P-type diffusion region 55 as the drain region is constructed. The P-type diffusion regions 54, 55 consist of P-type low concentration diffusion regions 54A, 55A, P-type middle concentration diffusion regions 54C, 55C, and P-type high concentration diffusion regions 54B, 55B respectively. The P-channel high breakdown voltage MOS transistor of the first 25

embodiment has the breakdown voltage of about 30 V.

Although their explanation will be omitted hereinbelow, a source electrode and a drain electrode are formed to come into contact with the N-type diffusion regions 4, 5 and the P-type diffusion regions 54, 55 after the overall surface has been covered with an interlayer insulating film.

A feature of the present invention resides in that the P-type middle concentration diffusion regions 54C, 55C (LP) constituting the P-type diffusion regions 54, 55 of the P-channel high breakdown voltage MOS transistor (B) can be formed by the same step as the ion-implantation step to form the P-type body region 3 in DMOS transistor forming steps when the N-channel LDMOS transistor (A) and the P-channel high breakdown voltage MOS transistor (B) are formed as above. Then, because such P-type middle concentration diffusion regions 54C, 55C are formed, the lower ON-resistance of the P-channel high breakdown voltage MOS transistor (B) can be achieved rather than the structure in the prior art. In addition, since the ion-implantation step in steps of manufacturing the N-channel LDMOS transistor (A) may be used as the concerned step, the number of manufacturing steps is never increased uselessly.

The method of manufacturing the semiconductor device mentioned above will be explained with reference to the drawings hereunder.

In FIG.2A, a P-type well 21 and an N-well 51 are formed in the P-type semiconductor substrate, then a pad oxide film 30 is formed thereon, and then first and second ion-implantation layers 32, 33 are formed by ion-implanting two kind N-type impurities (e.g., an arsenic ion and a phosphorus ion) while using a photoresist film

31, which has an opening portion 31a within the P-type well 21, as a mask so as to form the N⁻-type layer 22 acting as the drift region by the postprocessing. As the ion-implanting conditions of this step, for example, the arsenic ion is implanted by the accelerating voltage of about 160 KeV at a dose of $3 \times 10^{12} / \text{cm}^2$, and the phosphorus ion is implanted by the accelerating voltage of about 50 KeV at a dose of $4 \times 10^{12} / \text{cm}^2$.

Then, as shown in FIG.2B, the LOCOS oxide film 9 of about 7300 Å thickness is formed by selectively oxidizing the surface of the substrate with using a silicon nitride film 34 formed on the substrate 1 as a mask. Also, owing to difference in diffusion coefficients of the arsenic ion and the phosphorus ion which have been implanted into the surface layer of the substrate as described above, the arsenic ion is diffused into the substrate 1 and thus the first N⁻-type layer 22A is formed at a relatively shallow position in the surface layer of the substrate. Also, because the phosphorus ion is diffused into the substrate 1, the second N⁻-type layer 22B is formed at a relatively deep position in the P-type well region 21.

Then, in FIG.3A, a photoresist film 39 having opening portions 39a is formed in the source forming region in the P-type well region 21 and the source/drain forming region in the N-type well region 51 on the substrate 1, and then the P-type impurity (e.g., boron ion) is ion-implanted into the source forming region in the P-type well region 21 and the source/drain forming region in the N-type well region 51 on the surface layer of the substrate by using the photoresist film 39 as a mask and then diffused. Therefore, the second N⁻-type layer 22B in the source forming region can be

eliminated by canceling the phosphorus ion, which is employed to form the second N⁻type layer 22B in the source forming region, with the boron ion, and also the P-type low concentration diffusion regions 54A, 55A (P-) are formed in the source/drain forming region 5 of the P-channel high breakdown voltage MOS transistor (B). According to this step, for example, the P-type low concentration diffusion regions 54A, 55A (P-) are formed to have the concentration of about $1 \times 10^{17} / \text{cm}^3$ by implanting the boron ion by using the accelerating voltage of about 80 KeV at a dose of $8 \times 10^{12} / \text{cm}^2$ and 10 then annealing at 1100 °C for two hours. FIG.6 is a graph showing a concentration distribution when the arsenic ion (indicated by a solid line), the phosphorus ion (indicated by a dotted line), and the boron ion (indicated by a dot-dash line) are diffused respectively. As can be seen from FIG.6, the concentration distribution based on the phosphorus ion in the substrate is 15 overlapped with the concentration distribution based on the boron ion, and thus is canceled.

In this manner, in the present invention, since the boron ion being implanted by the postprocessing is diffused in forming 20 the drift region, the second N⁻layer 22B which is formed deeply in the substrate on the source forming region side can be canceled based on difference in diffusion coefficients of the arsenic ion and the phosphorus ion, so that only the first N⁻layer 22A formed in the surface layer of the substrate still remains on the source 25 forming region side. As a result, the N-channel LDMOS transistor (A) in which reduction in ON-resistance can be achieved can be provided by relatively simple manufacturing steps.

Then, in FIG.3B, first and second gate insulating films 6,

56 of about 800 Å thickness are formed on the substrate 1, then the
gate electrode 7 of about 2500 Å thickness is formed to extend over
the first gate insulating film 6 to the LOCOS oxide film 9, and then
the second gate electrode 57 of about 2500 Å thickness is formed
5 on the second gate insulating film 56, by forming a conductive film
on an entire surface and patterning them. In the first embodiment,
P-doped polycrystalline silicon film is used as the conductive film,
polyside film formed by forming a tungsten silicide(WSix) film on
the P-doped polycrystalline silicon film can be used as the
10 conductive film.

Then, in FIG.4A, a photoresist film 40 having opening
portions 40a is formed to cover the gate electrode 7 and the drain
forming region of the N-channel LDMOS transistor (A) and the P-
channel high breakdown voltage MOS transistor (B) other than a part
15 of the source/drain forming region. Then, the P-type body region
3 and the P-type middle concentration diffusion regions 54C, 55C
(LP) are formed by implanting the P-type impurity (e.g., boron ion)
while using the photoresist film 40 as a mask and then diffusing
it. The P-type body region 3 is located adjacent to one end of the
20 gate electrode 7, and the P-type middle concentration diffusion
regions 54C, 55C (LP) are located in a part of the source/drain
forming region of the P-channel high breakdown voltage MOS
transistor (B). According to this step, for example, the P-type
body region 3 and the P-type middle concentration diffusion regions
25 54C, 55C (LP) are formed to have the concentration of about $5 \times 10^{17} / \text{cm}^3$, by implanting the boron ion by using the accelerating
voltage of about 40 KeV at a dose of $5 \times 10^{13} / \text{cm}^2$ and then annealing
at 1050 °C for two hours.

Then, in FIG.4B, a photoresist film 41 having an opening portion 41a located over the source-forming region which is formed in the P-type body region 3 is formed. Then, the N-type lower concentration diffusion region 4A constituting the source region 5 of the N-channel LDMOS transistor (A) is formed by implanting the N-type impurity (e.g., phosphorus ion) while using the photoresist film 41 as a mask. According to this step, for example, the phosphorus ion is implanted by the accelerating voltage of about 40 KeV at a dose of $3.5 \times 10^{13} / \text{cm}^2$.

10 Then, in FIG.5A, sidewall spacer films 43 are formed to cover side wall portions of the first and second gate electrodes 7, 57. Then, a photoresist film 44 having an opening portion 44a which is located over the source/drain forming region of the N-channel LDMOS transistor (A) is formed. Then, the N-type high concentration 15 diffusion regions 4B, 5B (N+) constituting the source/drain region of the N-channel LDMOS transistor (A) by implanting the N-type impurity (e.g., arsenic ion) while using the photoresist film 44 as a mask. According to this step, for example, the arsenic ion is implanted by the accelerating voltage of about 80 KeV at a dose 20 of $5 \times 10^{15} / \text{cm}^2$.

Then, in FIG.5B, a photoresist film 45 having opening portions 45a is formed. Such opening portions 45a are located over the P-type diffusion region forming region, which supplies the potential to the P-type body region 3 and is adjacent to the N-type diffusion region 4, and a part of the source/drain forming 25 region of the P-channel high breakdown voltage MOS transistor (B) (at least in the region smaller than the P-type middle concentration diffusion regions 54C, 55C (LP)). Then, the P-type diffusion region

12 which is adjacent to the N-type diffusion region 4 and the P-type high concentration diffusion regions 54B, 55B (P+) which are located in the source/drain forming region of the P-channel high breakdown voltage MOS transistor (B) are formed by implanting the P-type 5 impurity (e.g., boron difluoride ion) while using the photoresist film 45 as a mask.

Subsequently, the interlayer insulating film is formed as in the configuration in the prior art, and then the source electrode and the drain electrode are formed via the interlayer

10 insulating film, whereby the semiconductor device can be completed.

As described above, according to the semiconductor device manufacturing method of the first embodiment of the present invention, since the N-type layer 22 serving as the drift region can be formed by using difference in diffusion coefficients of the 15 phosphorus ion, the arsenic ion which has the diffusion coefficient different from the phosphorus ion, and the boron ion which has the diffusion coefficient substantially identical to or larger than the phosphorus ion, the manufacturing steps can be made simple. In addition, since the phosphorus ion being located in the deep region 20 can be canceled by the boron ion upon forming the N-type shallow layer 22A serving as the drift region, the N-type layer 22A can be formed shallowly and its donor concentration Nd can be increased larger, and also the acceptor concentration Na in the P-well 21 located on the substrate side, i.e., at the junction portion can 25 be increased. Accordingly, the N-type shallow layer 22A can be put perfectly into the depletion layer by a low voltage, and then clamped at this low voltage. For this reason, even if the voltage higher than this low voltage is applied to the drain, the voltage

of the N⁻type shallow layer 22A is in no way changed. As a result, the higher breakdown voltage can be achieved rather than the N⁻type shallow layer which is formed by simply implanting the N⁻type impurity only into the P-well.

5 By the way, in order to achieve the higher breakdown voltage of the NchDMOS, it is needed that the N⁻type Resurf layer can be put perfectly into the depletion layer by the low voltage and then clamped at this low voltage. Once the N⁻type Resurf layer is clamped at a certain voltage, the voltage of the N⁻type Resurf layer 10 is not changed even if the voltage in excess of this voltage is applied to the drain.

Conversely, in order to reduce the ON-resistance, the 15 resistance of the N⁻type diffusion layer must be lowered by increasing the concentration of the N⁻type Resurf layer. In order to change perfectly the N⁻type diffusion layer of relatively high concentration into the depletion layer by the low voltage, it is effective to form the shallow junction. At the same time, it is effective to increase the concentration on the substrate side.

FIG.21 shows the dependency of the clamp (perfect depletion 20 state) voltage of the N⁻type Resurf layer upon the substrate concentration (here the acceptor concentration of the P-well: Na) if the junction between the N⁻type Resurf layer and the substrate is assumed as abrupt junction (FIG.22).

The clamp (perfect depletion state) voltage is detected when 25 the N⁻type layer is formed as the diffusion layer of $1 \times 10^{17} / \text{cm}^3$ and $X_j=0.2 \mu\text{m}$. It can be understood that, because of the increase of the substrate concentration (Na), the clamp (perfect depletion state) voltage can be lowered.

If this event is applied to the Nch LDMOS of the semiconductor device shown in FIG.1, it is possible to say the following. That is, the Resurf action can be produced at the lower voltage by increasing the substrate concentration by using the P-type layer (shown as a broken line in Fig.1) as well as forming the junction depth of the N-type layer at the shallow position. In this manner, since the shallow and high concentration drift region can be formed by implanting the acceptor impurity to cancel the donor impurity after the donor impurity has been implanted once, the higher breakdown voltage can be achieved rather than the case where the shallow drift region is formed by implanting shallowly the donor impurity.

Further, since the boron ion implanted to form the N-type layer 22 can be implanted by the same step as the ion-implanting step which is applied to form the P-type low concentration diffusion regions 54A, 55A (P-) constituting the P-type diffusion regions 54, 55 (P-) of the P-channel high breakdown voltage MOS transistor (B), the number of manufacturing steps is never increased in vain.

Furthermore, since the P-type middle concentration diffusion regions 54C, 55C(LP) constituting the P-type diffusion regions 54, 55 of the P-channel high breakdown voltage MOS transistor (B) can be formed by the same step as the ion-implanting step, which is applied to form the P-type body region 3, out of the LDMOS transistor forming steps employed when the N-channel LDMOS transistor (A) and the P-channel high breakdown voltage MOS transistor (B) are fabricated, the ON-resistance of the P-channel high breakdown voltage MOS transistor (B) can be further lowered rather than the structure in the prior art. Besides, since the ion-implanting step

of the steps of manufacturing the N-channel LDMOS transistor (A) can also be used as the present step, there is no situation that the number of manufacturing steps is increased meaninglessly.

FIG. 7 is a view showing a semiconductor device manufacturing method according to a second embodiment of the present invention. A feature of the second embodiment different from the first embodiment is a relation between the P-type low concentration diffusion regions 64A, 65A and the P-type high concentration diffusion regions 64B, 65B both constituting the P-type diffusion regions 64, 65 of the P-channel high breakdown voltage MOS transistor (B). That is, the P-type high concentration diffusion regions 64B, 65B are formed up to a depth which is deeper than the forming depth of the P-type low concentration diffusion regions 64A, 65A. And, like the first embodiment, the P-type middle concentration diffusion regions 64C, 65C are formed wider and deeper than the P-type high concentration diffusion regions 64B, 65B.

Next, a third embodiment of the present invention will be explained hereunder.

FIG. 8 is a sectional view showing an LDMOS transistor according to the third embodiment. The N-channel LDMOS transistor structure is shown as an example. Although the explanation of the P-channel LDMOS transistor structure is omitted, it is well known that such structure has the similar structure except for the different conductivity type. In this case, same symbols are affixed to constituent elements similar to those in the prior art, and their explanation will be simplified.

In FIG. 8, 1 denotes a conductivity type, e.g., P-type semiconductor substrate, and 21 denotes the P-type well region. The

N-type layer 22 as well as the P-type body region 3 is formed in the P-type well region 21. The N-type diffusion region 4 is formed in the P-type body region 3, and the N-type diffusion region 5 is formed in the N-type layer 22. The gate electrode 7 is formed on the surface of the substrate via the gate insulating film 6. The channel region 8 is formed in the surface region of the P-type body region 3 immediately below the gate electrode 7.

The N-type diffusion region 4 acts as the source region and the N-type diffusion region 5 acts as the drain region, and the N-type layer 22 under the first LOCOS oxide film 9A acts as the drift region.

In addition, a plurality of LDMOS transistors having the above structure are arranged via the second LOCOS oxide film 9B serving as the element isolation film, and a channel stopper layer 38 is formed under the second LOCOS oxide film 9B. Further the plurality of transistors arranged via the second LOCOS oxide film 9B serving as the element isolation film are not limited to the LDMOS transistors described as above, and the present invention is applicable to a LDMOS transistors having the above structure and a MOS transistor having a high breakdown voltage arranged via the second LOCOS oxide film 9B serving as the element isolation film.

A feature of the third embodiment resides in that the channel stopper layer 38 is formed under the second LOCOS oxide film 9B in the structure in which a plurality of LDMOS transistors having the above structure are arranged via the second LOCOS oxide film 9B serving as the element isolation film.

Further, spread of the depletion layer in the diffusion regions 4, 5 of the LDMOS transistors which are positioned

adjacently via the second LOCOS oxide film 9B can be suppressed by the channel stopper layer 38 formed under the second LOCOS oxide film 9B. Therefore, the second LOCOS oxide film 9B per se can be reduced in size and thus the higher integration can be achieved.

5 In addition, the higher integration is made possible by employing the N'-type layer 22 in place to the N'-type layer 22 in the prior art structure. According to such structure, a size of the second LOCOS oxide film 9B per se can be reduced up to the size L1 (about 10 μm to 30 μm) (the conventional size L2 is about 10 μm to 30 μm).

10 Besides, the higher breakdown voltage can be achieved by increasing a distance from an end portion of the second LOCOS oxide film 9B to the channel stopper layer 38 up to about 2 μm to 3 μm .

15 FIGS.8 to 16 are views showing steps of manufacturing a plurality of LDMOS transistors.

These steps are almost similar to those shown in FIGS.2 to 5 in the first embodiment. However, in FIG.10, a second photoresist film 36 is formed on the substrate 1 to cover a silicon nitride film 34 which is patterned via a first photoresist film 35, and then a 20 channel stopper layer forming ion-implantation layer 37 is formed by ion-implanting the P-type impurity (e.g., boron ion) into a certain region of the substrate surface (forming region in which a channel stopper layer 38 is formed by the postprocessing) while using the second photoresist film 36 as a mask. According to this 25 step, for example, the boron ion is implanted by the accelerating voltage of about 60 KeV at a dose of $5 \times 10^{13} / \text{cm}^2$. Then, since the ion implantation to form the channel stopper layer of the LDMOS transistor is carried out by the same step as the step of forming

the channel stopper layer formed in the normal high breakdown MOS transistor, the number of manufacturing steps is never increased in vain.

Because remaining steps correspond to those in the first 5 embodiment, their explanation will be omitted. In the third embodiment, the higher breakdown voltage can be attained by increasing the distance from an end portion of the second LOCOS oxide film 9B to the channel stopper layer 38 up to about $2 \mu\text{m}$ to $3\mu\text{m}$.

10 According to this method, in addition to the advantage achieved by the above first embodiment, the number of manufacturing steps is never increased since the step of forming the channel stopper layer 38 can be carried out simultaneously with the step of forming the channel stopper layer of the normal high breakdown 15 voltage MOS transistor.

FIG.17 is a sectional view showing a semiconductor device according to a fourth embodiment of the present invention. A feature of the fourth embodiment different from the foregoing third embodiment is that the diffusion regions 4, 5 of a plurality of LDMOS 20 transistors being arranged via the element isolation film 9B are reversely arranged. The further higher integration can be achieved by employing such arrangement. More particularly, because the diffusion region (source region) 4 has the fixed potential, the element isolation film 9B can be reduced in size in the configuration 25 in which the diffusion region (source region) 4 and the diffusion region (drain region) 5 are positioned adjacently rather than the configuration in which the diffusion regions (drain regions) 5 whose potential is varied are positioned adjacently via the element

isolation film 9B.

It is needless to say that the above feature to enable the high integration is effective if such feature is applied to the LDMOS transistor having the conventional structure, i.e., the N-type well 5 region 2 is formed uniformly up to the same depth position.

Industrial Applicability

According to the semiconductor device of the present invention, since the low concentration layer serving as the drift region is formed shallowly at least under the gate electrode but 10 formed deeply in the neighborhood of the drain region, the higher breakdown voltage and reduction in the ON-resistance can be achieved. Since the drift region can be formed by using difference in diffusion coefficients of the phosphorus ion, the arsenic ion which has the diffusion coefficient different from the phosphorus ion, and the 15 boron ion which has the diffusion coefficient substantially identical to or larger than the phosphorus ion, the manufacturing steps can be made simple. In addition, since the boron ion implanted to form this drift region can be implanted by the same step as the ion-implanting step which is applied to form the P-type low 20 concentration diffusion regions of the P-channel high breakdown voltage MOS transistor, the number of manufacturing steps is never increased in vain.

In the case that a plurality of semiconductor devices having the above structure are arranged via the element isolation film, 25 a size of the element isolation film can be reduced and high integration can be achieved by forming a channel stopper under the element isolation film.

Further since a channel stopper layer can be formed by the

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same step as the step of forming a channel stopper of the MOS transistor having a high breakdown voltage, the number of manufacturing steps is never increased in vain.

In addition, since the P-type middle concentration diffusion regions of the P-channel high breakdown voltage MOS transistor can be formed by utilizing the DMOS transistor forming steps employed when the N-channel LDMOS transistor and the P-channel high breakdown voltage MOS transistor are fabricated, the lower ON-resistance can be achieved in the P-channel high breakdown voltage MOS transistor rather than the structure in the prior art.

Moreover, since the ion-implanting step of the steps of manufacturing the N-channel LDMOS transistor can also be utilized as the step of forming the P-type middle concentration diffusion regions, the number of manufacturing steps are in no means increased uselessly.

What is Claimed is:

1 1. A semiconductor device comprising a source region, a channel
2 region, a drain region, a gate electrode formed on the channel region,
3 and a drift region formed between the channel region and the drain
4 region,

5 wherein the drift region is formed shallowly at least below
6 the gate electrode but formed deeply in a neighborhood of the drain
7 region.

1 2. A semiconductor device comprising:

2 a first conductivity type well region formed in a first
3 conductivity type semiconductor substrate;
4 a gate electrode formed on the substrate via a gate insulating
5 film;

6 a first conductivity type body region formed to be adjacent
7 to the gate electrode;

8 a second conductivity type source region and a channel region
9 formed in the first conductivity type body region;

10 a second conductivity type drain region formed at a position
11 remote from the first conductivity type body region; and

12 a second conductivity type drift region formed shallowly from
13 the channel region to the drain region, at least below the gate
14 electrode, and formed deeply in a neighborhood of the drain region.

1 3. A semiconductor device according to claim 2, wherein the
2 second conductivity type drift region is formed by implanting at
3 least two kind second conductivity type impurities which have

4 different diffusion coefficients and at least one kind first
5 conductivity type impurity which has a diffusion coefficient
6 substantially equal to or larger than the diffusion coefficient of
7 at least one kind second conductivity type impurity such that it
8 is formed by diffusing the second conductivity type impurities into
9 a deep region by using a difference in the diffusion coefficients
10 and is formed shallowly in a neighborhood of the source region by
11 canceling the second conductivity type impurities by the first
12 conductivity type impurity.

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1 4. A semiconductor device according to claim 3, wherein the
2 second conductivity type drift region is formed by implanting an
3 arsenic ion and a phosphorus ion as the second conductivity type
4 impurities into an overall surface of a region serving as the drift
5 region and selectively implanting a boron ion as the first
6 conductivity type impurity only into a region in a neighborhood of
7 the source region.

1 5. A method of manufacturing a semiconductor device including
2 a first conductivity type well region formed in a first conductivity
3 type semiconductor substrate, a gate electrode formed on the
4 substrate via a gate insulating film, a first conductivity type body
5 region formed to be adjacent to the gate electrode, a second
6 conductivity type source region and a channel region formed in the
7 first conductivity type body region, a second conductivity type
8 drain region formed at a position remote from the first conductivity
9 type body region, and a second conductivity type drift region formed
10 shallowly from the channel region to the drain region, at least below

11 the gate electrode, and formed deeply in a neighborhood of the drain
12 region,

13 wherein the steps of forming the drift region, comprising
14 the steps of:

15 implanting two kind second conductivity type impurities to
16 form a second conductivity type low concentration layer
17 constituting the drift region in the first conductivity type well
18 region in the first conductivity type semiconductor substrate via
19 postprocessing;

20 implanting selectively the first conductivity type impurity
21 into a region located in a neighborhood of the source region; and

22 diffusing impurities under a condition that a diffusion
23 coefficient of the first conductivity type impurity is set equal
24 to or larger than a larger one of diffusion coefficients of the second
25 conductivity type impurities.

1 6. A method of manufacturing a semiconductor device,
2 comprising the steps of:

3 ion-implanting two kind second conductivity type impurities
4 to form a second conductivity type low concentration layer serving
5 as a drift region in a first conductivity type well region in a first
6 conductivity type semiconductor substrate via postprocessing;

7 forming a LOCOS oxide film by oxidizing selectively a certain
8 region on the substrate, and forming the second conductivity type
9 low concentration layer at a relatively deep position in the first
10 conductivity type well region and on a surface layer of the substrate
11 by using a difference in diffusion coefficients of two kind second
12 conductivity type impurities respectively;

13 ion-implanting and diffusing a first conductivity type
14 impurity into the surface layer of the substrate of a source forming
15 region via a mask which is formed on a drain forming region on the
16 substrate so as to cancel the second conductivity type layer formed
17 at the relatively deep position in the first conductivity type well
18 region of the source forming region by a diffusion of the first
19 conductivity type impurity;

20 forming a gate insulating film on the substrate, then forming
21 a gate electrode to extend from the gate insulating film to the LOCOS
22 oxide film, and then forming a first conductivity type body region
23 adjacently to one end portion of the gate electrode by implanting
24 and diffusing the first conductivity type impurity via a mask which
25 is formed to cover the gate electrode and the drain forming region;
26 and

27 forming a source/drain region by implanting the second
28 conductivity type impurities via a mask having opening portions
29 which are located over the source forming region and the drain
30 forming region being formed in the first conductivity type body
31 region.

1 7. A method of manufacturing a semiconductor device,
2 according to claim 6, wherein the second conductivity type low
3 concentration layer serving as the drift region is formed by
4 implanting two kind second conductivity type impurities which have
5 different diffusion coefficients and the first conductivity type
6 impurity which has a diffusion coefficient substantially equal to
7 or larger than the diffusion coefficient of one kind second
8 conductivity type impurity of two kind second conductivity type

9 impurities such that it is formed by diffusing the second
10 conductivity type impurities into a deep region by using a
11 difference in the diffusion coefficients and also formed shallowly
12 in a neighborhood of the source region by canceling the second
13 conductivity type impurities by the first conductivity type
14 impurity.

1 8. A semiconductor device comprising a first MOS transistor
2 having a source region, a channel region, a drain region, a gate
3 electrode formed on the channel region, and a drift region formed
4 between the channel region and the drain region, and a second MOS
5 transistor having a source region, a channel region, a drain region,
6 and a gate electrode formed on the channel region,
7 wherein the drift region of the first MOS transistor is
8 formed shallowly at least below the gate electrode but formed deeply
9 in a neighborhood of the drain region and
10 a source/drain region of the second MOS transistor consists
11 of a low concentration source-drain region, a high concentration
12 source-drain region, and a middle concentration source/drain region
13 whose concentration is higher than that of the low concentration
14 source/drain region but lower than that of the high concentration
15 source/drain region.

1 9. A semiconductor device comprising a first MOS transistor
2 and a second MOS transistor formed on a first conductivity type
3 semiconductor substrate;
4 wherein the first MOS transistor includes,
5 a first conductivity type well region formed in the

6 semiconductor substrate,
7 a first gate electrode formed on the first conductivity
8 type well region via a first gate insulating film,
9 a first conductivity type body region formed to be
10 adjacent to the first gate electrode,
11 a second conductivity type source region and a channel
12 region formed in the first conductivity type body region,
13 a second conductivity type drain region formed at a
14 position remote from the first conductivity type body region, and
15 a second conductivity type drift region formed
16 shallowly from the channel region to the drain region, at least below
17 the gate electrode, and formed deeply in a neighborhood of the drain
18 region, and
19 wherein the second MOS transistor includes,
20 a second conductivity type well region formed in the
21 semiconductor substrate,
22 a second gate electrode formed on the second
23 conductivity type well region via a second gate insulating film,
24 and
25 a source/drain region consisting of a low
26 concentration source/drain region formed to be adjacent to the
27 second gate electrode, a high concentration source/drain region,
28 and a middle concentration source/drain region whose concentration
29 is higher than that of the low concentration source/drain region
30 but lower than that of the high concentration source/drain region.

1 10. A semiconductor device according to claim 9, wherein the
2 first MOS transistor consists of an N-channel LDMOS transistor, and

3 the second MOS transistor consists of a P-channel high breakdown
4 voltage MOS transistor.

1 11. A method of manufacturing a semiconductor device which
2 includes a first MOS transistor having a body region in which a source
3 region and a channel region are formed, a drain region separated
4 from the body region, a gate electrode formed on the channel region,
5 and a drift region formed between the channel region and the drain
6 region, and a second MOS transistor having a source region, a channel
7 region, a drain region, and a gate electrode formed on the channel
8 region,

9 steps of forming a source/drain region of the second MOS
10 transistor comprising at least a same step as the step of forming
11 the body region of the first MOS transistor.

1 12. A method of manufacturing a semiconductor device,
2 according to claim 11, wherein the step of forming the source/drain
3 region of the second MOS transistor has at least a same step as the
4 step of forming the drift region.

1 13. A method of manufacturing a semiconductor device
2 according to claim 11, in which a first MOS transistor and a second
3 MOS transistor are formed on a first conductivity type semiconductor
4 substrate, comprising the steps of:

5 ion-implanting two kind second conductivity type impurities
6 having a different diffusion coefficient via a mask which has an
7 opening portion over a part of a first conductivity type well region
8 on a first conductivity type semiconductor substrate on which the

9 first conductivity type well region and a second conductivity type
10 well region are formed;

11 forming an oxidation resisting film in a certain region on
12 the substrate, then forming a LOCOS oxide film by oxidizing
13 selectively the substrate while using the oxidation resisting film
14 as a mask, and forming second conductivity type low concentration
15 layers at a relatively deep position in the first conductivity type
16 well region and on a surface layer of the substrate by using a
17 difference in diffusion coefficients of two kind second
18 conductivity type impurities respectively;

19 ion-implanting and diffusing a first conductivity type
20 impurity into a source forming region in the first conductivity type
21 well region and the surface layer of the substrate in a source/drain
22 forming region in the second conductivity type well region via a
23 mask, which has opening portions over the source forming region in
24 the first conductivity type well region and the source/drain forming
25 region in the second conductivity type well region, so as to cancel
26 the second conductivity type layer formed at the relatively deep
27 position in the source forming region in the first conductivity type
28 well region by a diffusion of the first conductivity type impurity
29 and to form a first conductivity type source/drain region in the
30 source/drain forming region in the second conductivity type well
31 region;

32 forming a first gate insulating film in a region other than
33 the LOCOS oxide film on the first conductivity type well region,
34 and forming a second gate insulating film in a region other than
35 the LOCOS oxide film on the second conductivity type well region;

36 forming a first gate electrode and a second gate electrode

37 on the first gate insulating film and the second gate insulating
38 film respectively;

39 ion-implanting and diffusing the first conductivity type
40 impurity via a mask, which covers the first gate electrode in the
41 first conductivity type well region and the drain forming region
42 and has an opening portion over a part of the source/drain forming
43 region on the second conductivity type well region, so as to form
44 a first conductivity type body region adjacently to one end portion
45 of the first gate electrode and to form a second first conductivity
46 type source/drain region in a region separated from the second gate
47 electrode;

48 forming a first second conductivity type source region by
49 implanting the second conductivity type impurities via a mask having
50 an opening portion located over the source forming region in the
51 first conductivity type well region;

52 forming sidewall spacer films on side wall portions of the
53 first gate electrode and the second gate electrode, and then forming
54 a second first conductivity type source/drain region by implanting
55 the first conductivity type impurity via a mask having an opening
56 portion located over the source/drain forming region in the first
57 conductivity type well region; and

58 forming a third first conductivity type source/drain region
59 by implanting the first conductivity type impurity via a mask having
60 at least an opening portion, which is smaller than the second first
61 conductivity type source/drain region, located over the second
62 conductivity type well region.

2 according to claim 13, wherein the second conductivity type low
3 concentration layer is formed by utilizing a difference in diffusion
4 coefficients between two type second conductivity type impurities
5 having a different diffusion coefficient and the first conductivity
6 impurity having a diffusion coefficient which is almost equal to
7 or larger than a diffusion coefficient of one of the second
8 conductivity type impurities.

1 15. A method of manufacturing a semiconductor device
2 according to claim 13, wherein concentration of the second first
3 conductivity type source/drain region is set to a middle
4 concentration which is higher than a concentration of the first
5 conductivity type source/drain region but lower than a
6 concentration of the third first conductivity type source/drain
7 region.

1 16. A method of manufacturing a semiconductor device
2 according to claim 11, wherein the first MOS transistor consists
3 of an N-channel LDMOS transistor, and the second MOS transistor
4 consists of a P-channel high breakdown voltage MOS transistor.

1 17. A semiconductor device according to claim 1, wherein the
2 semiconductor device is arranged in plural via a element isolation
3 film, and
4 a channel stopper layer is formed under the element isolation
5 film.

1 18. A method of manufacturing a semiconductor device

2 according to claim 6, further comprising the steps of:
3 ion-implanting two kind second conductivity type impurities
4 to form the second conductivity type low concentration layer serving
5 as the drift region in the first conductivity type well region in
6 the first conductivity type semiconductor substrate via
7 postprocessing;
8 forming an oxidation resisting film on the substrate, and
9 then ion-implanting the first conductivity type impurity into a
10 surface of the substrate via a mask which is formed to cover the
11 oxidation resisting film;
12 forming a first LOCOS oxide film and a second LOCOS oxide
13 film by oxidizing selectively certain regions on the substrate while
14 using the oxidation resisting film as a mask, and forming the second
15 conductivity type low concentration layer at a relatively deep
16 position in the first conductivity type well region and on a surface
17 layer of the substrate respectively by using a difference in
18 diffusion coefficients of two kind second conductivity type
19 impurities, and then forming a channel stopper layer under the
20 second LOCOS oxide film;
21 ion-implanting and diffusing the first conductivity type
22 impurity into the surface layer of the substrate in the source
23 forming region via a mask which is formed in the drain forming region
24 on the substrate so as to cancel the second conductivity type layer
25 formed at the relatively deep position in the first conductivity
26 type well region in the source forming region by the diffusion of
27 the first conductivity type impurity;
28 forming the gate insulating film in a region other than the
29 first LOCOS oxide film and the second LOCOS oxide film on the

30 substrate, then forming the gate electrode to extend from the gate
31 insulating film to the first LOCOS oxide film, and then forming the
32 first conductivity type body region adjacently to one end portion
33 of the gate electrode by implanting and diffusing the first
34 conductivity type impurity via a mask which is formed to cover the
35 gate electrode and the drain forming region; and
36 forming the source/drain region by implanting the second
37 conductivity type impurities via a mask having opening portions
38 which are located over the source forming region and the drain
39 forming region formed in the first conductivity type body region.

ABSTRACT

In order to improve the characteristics of the high breakdown voltage MOS transistor, a semiconductor device of the present invention is characterized in that an LDMOS transistor, which 5 comprises a source region 4, a channel region 8, and a drain region 5, and a gate electrode 7 formed on the channel region 8, and a drift region formed between the channel region 8 and the drain region 5, wherein an N⁻type low concentration layer 22 serving as the drift region is formed shallowly at least below the gate electrode 7 (first 10 N⁻type layer 22A) but formed deeply in a neighborhood of the drain region 5 (second N⁻type layer 22B).

FIG.1

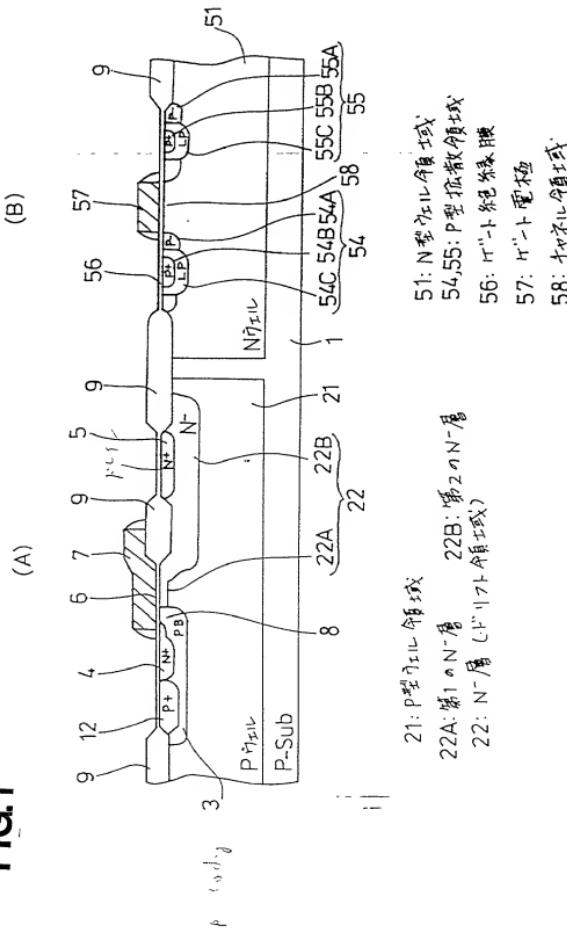
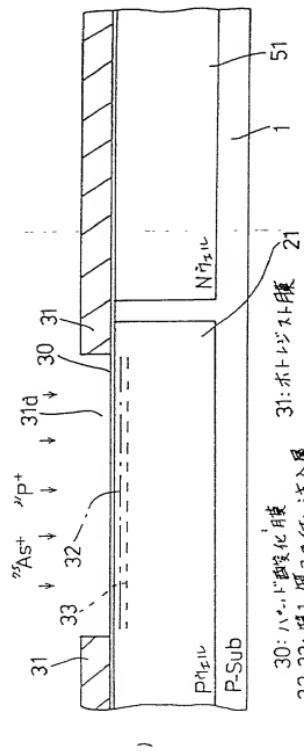


FIG. 2A



(A)

(B)

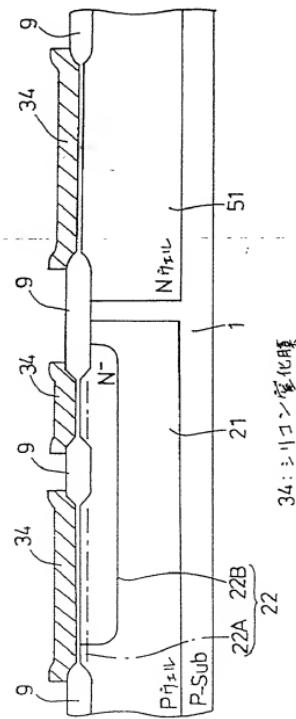


FIG. 2B

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整理番号=KIA0980196

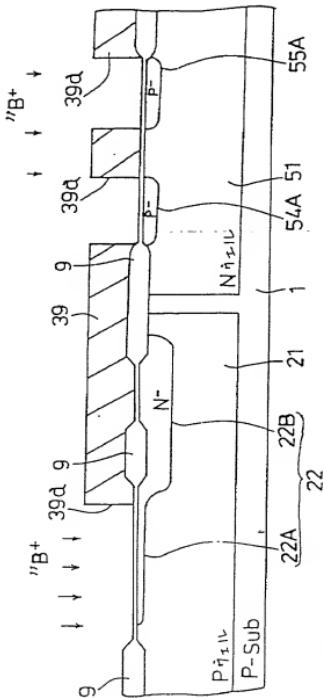


FIG 3A

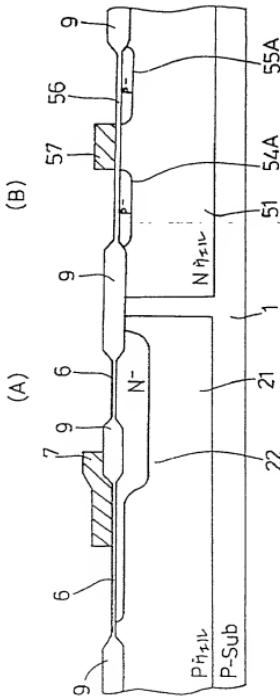


FIG. 3B

整理番号=KIA0980196

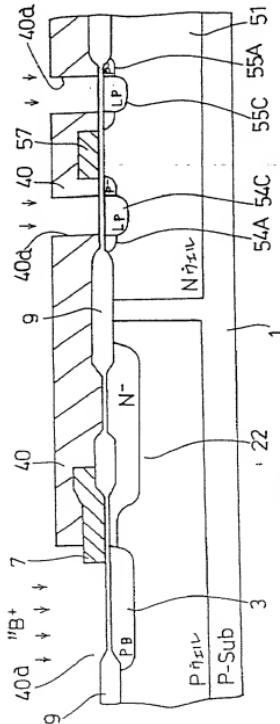


FIG.4A

40: ノトレジスト構成

(A)

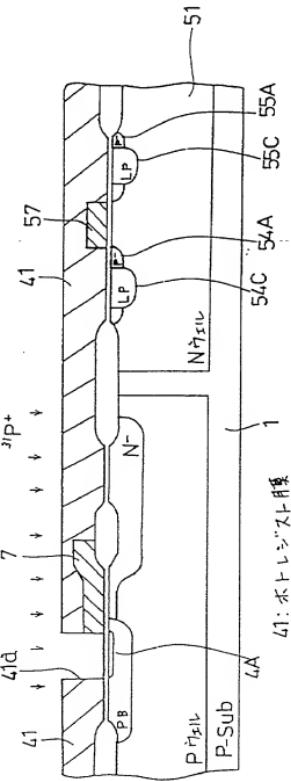


FIG.4B

41: ノトレジスト構成

ପାତା ୫

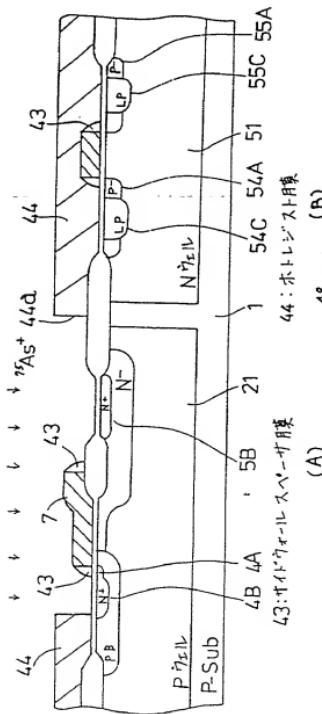


FIG. 5A

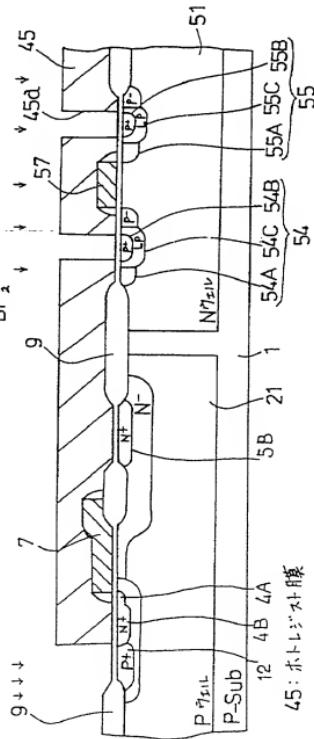


FIG. 5B

6/22

提出日 平成10年12月10日

整理番号=KIA0980196

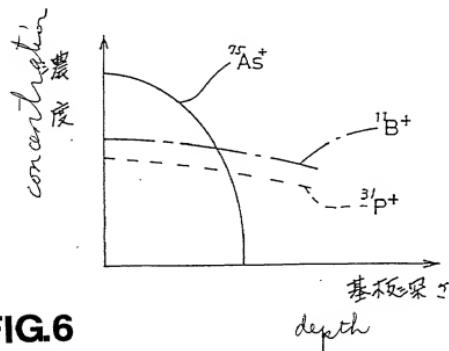
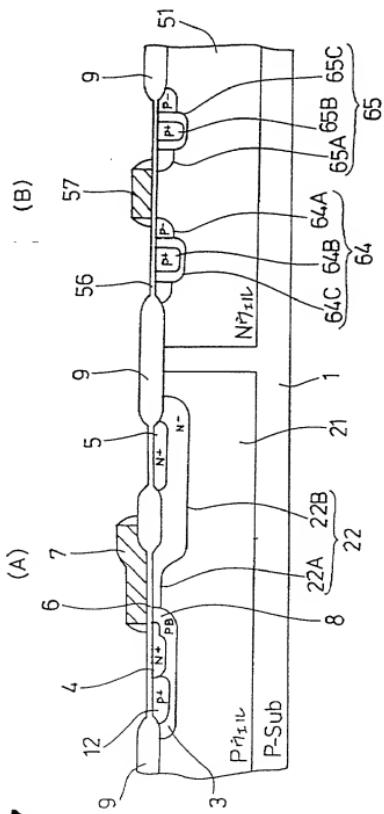


FIG.6

FIG.7



64,65: ライン命令区域

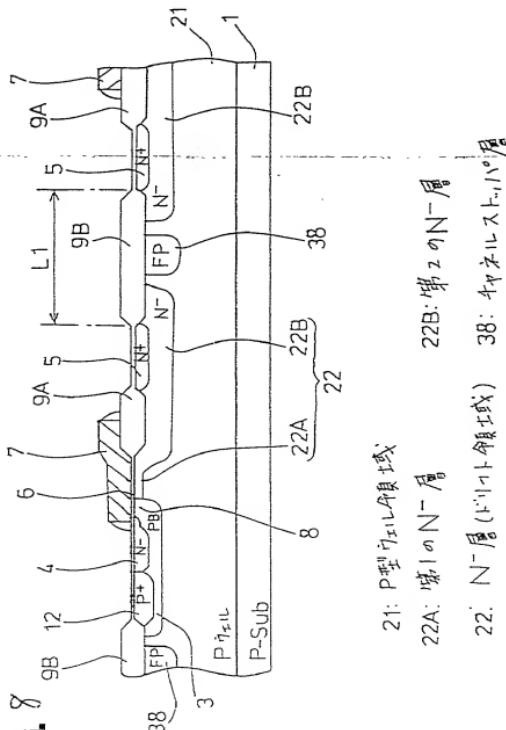
8/22

提出日 平成10年12月4日

整理番号=KIA0980186

【音譜名】 因回

[図1]
8

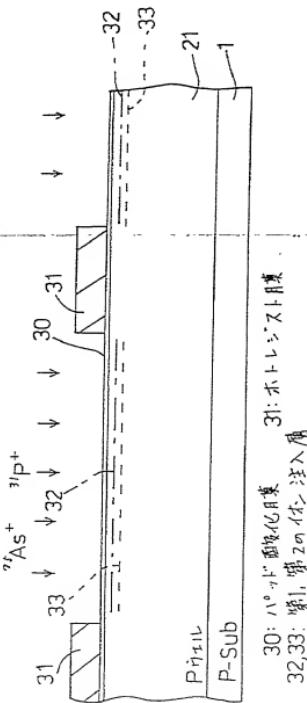


8
FIG

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提出日 平成10年12月 4日

FIG.9



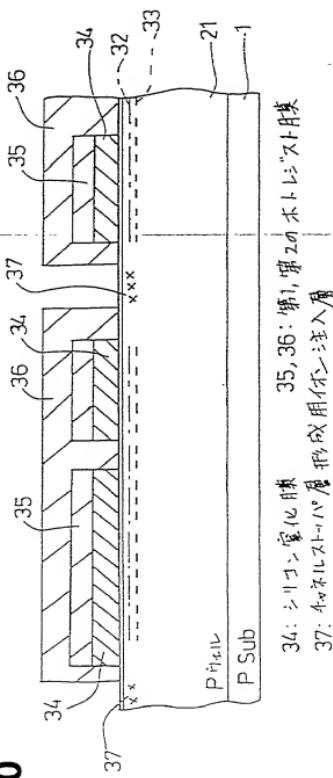
10/22

提出日 平成10年12月4日

整理番号=KIA0980186

10

FIG.10



34: ヒートシンク実化膜
 35, 36: 第1, 第2の木工ヒートシンク
 37: 4-πルーブルの層
 形成用作成入層

11/22

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登録番号=KIA0980186

11

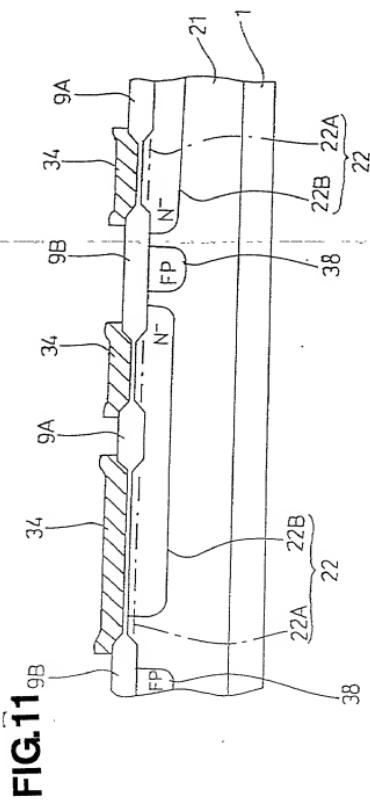


FIG. 11

12/22

提出日 平成10年12月4日

整理番号 = K I A 0 9 8 0 1 8 6

12

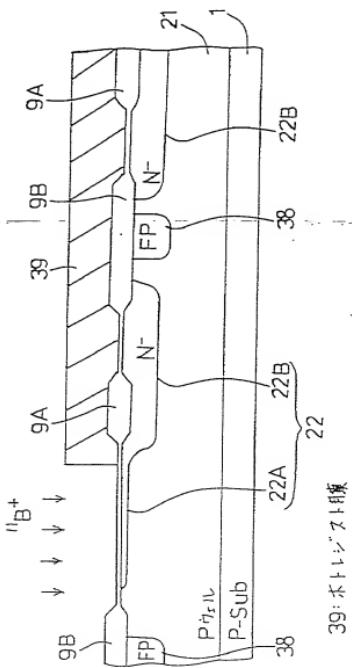


FIG. 12

13/22

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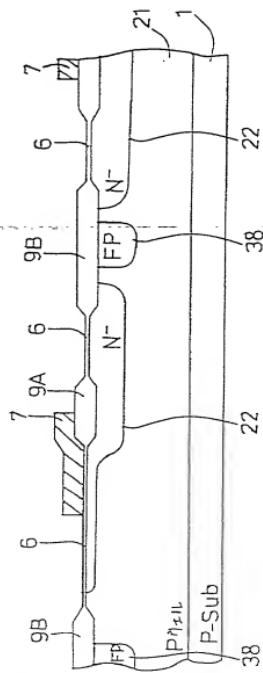


FIG.13

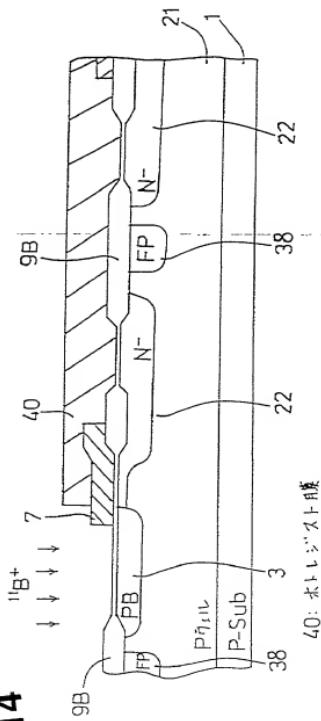
14/22

提出日 平成10年12月 4日

整理番号=KIA0980186

14

FIG.14

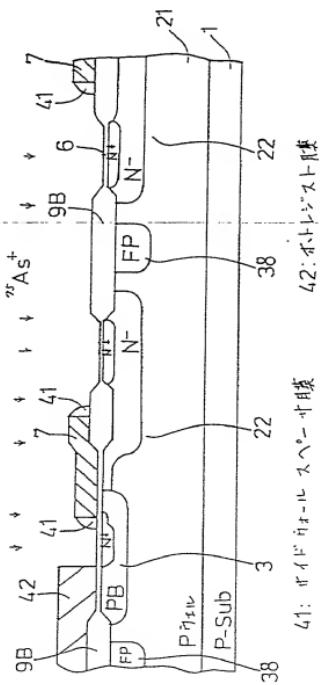


15/22

提出日 平成10年12月 4日

整理番号 = KIA0980186

15



61: 望天樹

42: 九、十一、十二、一月

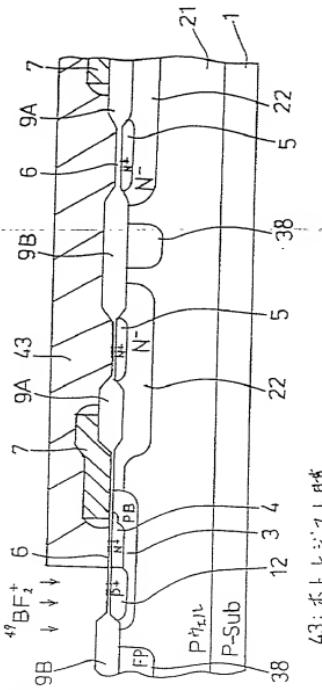
FIG. 15

16/22

整理番号=KIA0980186

提出日 平成10年12月 4日

16



43: ホトレジスト膜

FIG.16

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提出日 平成10年12月 4日

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17

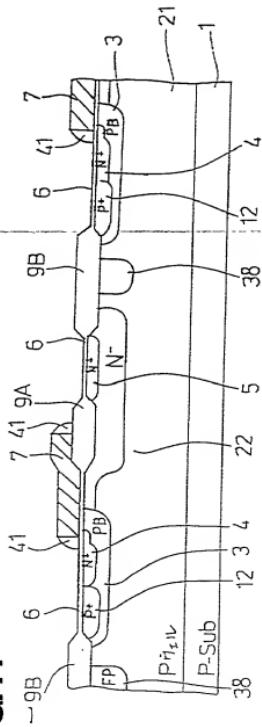


FIG.17

18/22

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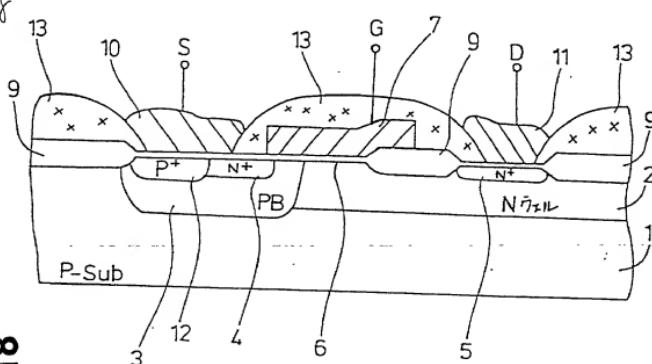


FIG.18

19/22

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整理番号=KIA0980196

FIG.19A

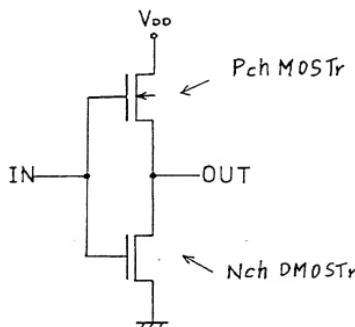
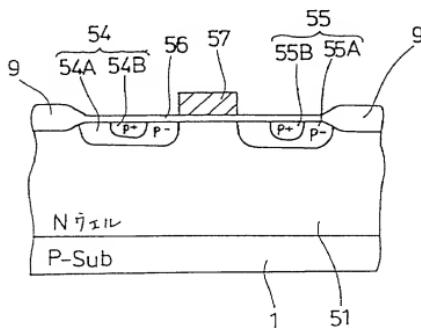


FIG.19B



20/22

提出日 平成10年12月 4日

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【図1-2】

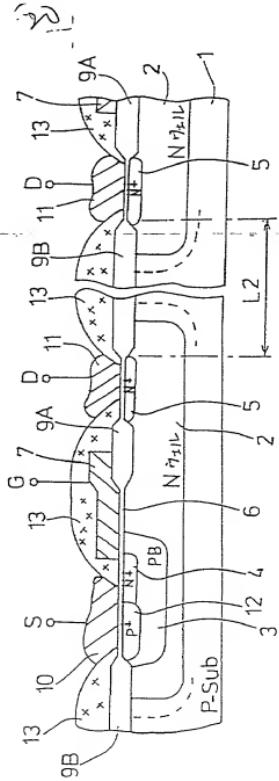
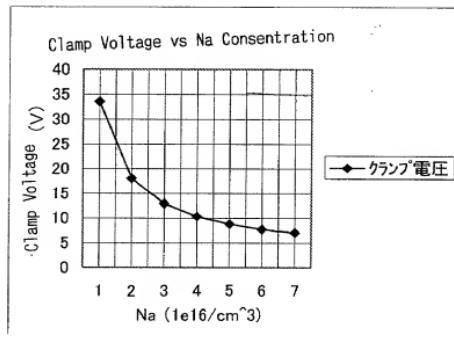


FIG.20

**FIG.21**

N-Clamp Voltage vs Na Concentration
Stepped Junction N-Concentration $10^{17}/\text{cm}^3$
 $X_j = 0.2 \mu\text{m}$

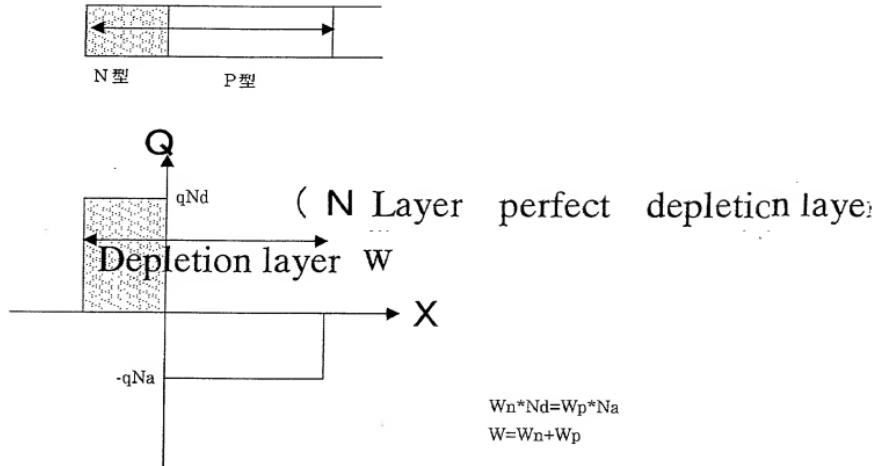


Fig.22 Stepped Junction

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、郵便番、国籍は下記の私の氏名の後に記載され
た通りです。

My residence, post office address and citizenship are as stated
next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願
している発明内容について、私が最初かつ唯一の発明者（下
記の氏名が一つの場合）もしくは最初かつ共同発明者である
と（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole Inventor (if only one name
is listed below) or an original, first and joint Inventor (if plural
names are listed below) of the subject matter which is claimed and
for which a patent is sought on the invention entitled

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

上記発明の明細書（下記の横でx印がついていない場合は、
本書に添付）は、

the specification of which is attached hereto unless the following
box is checked:

一月____日に提出され、米国出願番号または特許協定条約
国際出願番号を_____とし、
(該当する場合) _____に訂正されました。

was filed on _____
as United States Application Number or
PCT International Application Number
and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、
内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of
the above identified specification, including the claims, as
amended by any amendment referred to above.

私は、連邦規則法典第37篇第1条56項に定義される
おり、特許実務の有無について重要な情報を開示する義務が
あることを認めます。

I acknowledge the duty to disclose information which is material to
patentability as defined in Title 37, Code of Federal Regulations,
Section 1.56.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第35編119条(a)-(d)項又は365条(b)項に基づき下記の、米国以外の国の少なくとも一ヶ国を指定している特許協力条約365条(a)項に基づき出願提出し、又は外国での特許出願もしくは発明者証の提出についての外国優先権をここに主張することも、優先権を主張している、不出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

Prior Foreign Application(s)

外國での先行出願

P.Hei.10-335877	Japan
(Number) (番号)	(Country) (国名)
P.Hei.10-345651	Japan
(Number) (番号)	(Country) (国名)

私は、第35編米国法119条(a)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

(Application No.) (出願番号)	(Filing Date) (出願日)
-----------------------------	------------------------

私は、下記の米国法典第35編120条に基いて下記の米国特許出願に記載された権利、又は米国を相手にしている特許協力条約365条(c)に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約に規定された方針で示する米国特許出願に記載されていない限り、その先行米国特許出願提出日以降で本出願書の日本国または特許協力条約の当事国出願書での発明内容が本特許協力条約に規定された方針で示する米国法典第35編119条(a)項及び365条(b)に記載された特許の有効性に関する重要な情報について認示義務があることを認識しています。

(Application No.) (出願番号)	(Filing Date) (出願日)
-----------------------------	------------------------

私は、私自身の知識に基いて本宣言書でなが行なう声明が真実であり、かつ私の入手した情報と私の信じるところに基づく表明が全て真実であるとはじていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認定し、よってここに上記のごとく宣言を致します。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 364(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Priority Not Claimed

優先権主張なし

26/November/1998

(Day/Month/Year Filed)

04/December/1998

(Day/Month/Year Filed)

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)
-----------------------------	------------------------

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 364(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.66 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Status: Patented, Pending, Abandoned) (現況: 特許可済、候査中、放棄済)
--

(Status: Patented, Pending, Abandoned) (現況: 特許可済、候査中、放棄済)
--

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

私は、米国特許第3,545,119号(a)-(d)項又は3,654,616号(b)項に基いて下記の、米国以外の国々の少なくとも二ヶ国を指定している特許協力条約3,655(a)項に基づく出願出願、又は他のどの特許出願もしくは発明者証の並びについての外国优先権をここに主張することとし、優先権を主張している、本出願の前に出願された特許または発明者証の外國出願を以下に、番号をマークすることで、示していきます。

Prior Foreign Application(s)

外国での先行出願

P. Bei.10-351779

(Number)

(番号)

Japan

(Country)

(国名)

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 364(b) of any foreign application(s) for patent or inventor's certificate, or 35(e) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Priority Not Claimed

既先権主張なし



10/December/1998

(Day/Month/Year Filed)

(出願年月日)

(Day/Month/Year Filed)

(出願年月日)

私は、第3,545,119号(e)項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

(Application No.)

(出願番号)

(Filing Date)

(出願日)

(Application No.)

(出願番号)

(Filing Date)

(出願日)

私は、下記の米国特許第3,545,120号と並んで下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約3,655(c)項に基づく権利をここに主張します。また、本出願の各請求項の内容が米国特許第3,545,119号第1項又は若者協力条約で記載された出願で発行する米国特許出願に表示されていない限り、その出願米国出願番号出日以降で本出願番号の日本出願内または特許協力条約出願出日までの期間中に入手された、運営販売業者第3,741,155号と並記された特許出願の著者に関する主張の取消について開示義務があることを認めていきます。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.)

(出願番号)

(Filing Date)

(出願日)

(Application No.)

(出願番号)

(Filing Date)

(出願日)

(Application No.)

(出願番号)

(Filing Date)

(出願日)

(Status: Patented, Pending, Abandoned)

(現況: 特許可済、候査中、放棄済)

(Status: Patented, Pending, Abandoned)

(現況: 特許可済、候査中、放棄済)

私は、私自身の在りに基づいて本宣言書で私が行なう声明が真実であり、かつ私の入手した情報と私の信じるところに基づく差別が全て真実であると信じてのこと、さらに故意になされた虚偽の表明及びそれと同の行はに米国特許第1,842,001号に基づき、到会または否示、もしくはその反方に上り取消されること、そしてそのような故意による虚偽の声明を行なへば、出所した、又は蓋に許可された出願の有効性が失われることを認識し、よってここに上記のごとく宣言を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

委任状： 私は下記の発明者として、本出願に關する一切の手続を米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。（弁理士、または代理人の氏名及び登録番号を明記のこと）

POWER OF ATTORNEY: As a named Inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number)

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（第三以降の共同発明者についても同様に記載し、署名をすること）

(Supply similar information and signature for third and subsequent joint inventors.)